Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-105 (canceled)

106. (previously presented) A semiconductor chip or wafer comprising:

a silicon substrate;

a metallization structure over said silicon substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material;

a polymer layer over said passivation layer, wherein said polymer layer has a thickness of between 2 and 50 μm; and

a metal trace over part of said polymer layer and over said first contact pad, wherein said metal trace comprises a gold layer with a thickness of between 2 and 100 μm, and wherein said metal trace comprises a second contact pad connected to said first contact pad, wherein the positions of said first and second contact pads from a top perspective view are different.

107. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

108. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

109. (previously presented) The semiconductor chip or wafer of claim 106, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

110. (previously presented) The semiconductor chip or wafer of claim 106, wherein said metal trace further comprises a titanium-containing layer under said gold layer.

Claim 111 (canceled)

112. (previously presented) The semiconductor chip or wafer of claim 106, wherein said second contact pad is used to be wirebonded thereto.

113. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a circuit interconnect wirebonded to said second contact pad.

114. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a metal bump over said second contact pad.

115. (previously presented) The semiconductor chip or wafer of claim 106 further comprising a solder bump over said second contact pad.

116. (previously presented) The semiconductor chip or wafer of claim 106, wherein no polymer layer is over said metal trace.

Claims 117 and 118 (canceled)

119. (previously presented) The semiconductor chip or wafer of claim 106, wherein said gold layer is electroplated.

120. (currently amended) A semiconductor chip or wafer comprising:

a silicon substrate;

a metallization structure over said silicon substrate;

a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material; ~~and~~

a second contact pad connected to said first contact pad, wherein said second contact pad comprises a gold layer with a thickness of between 2 and 15 μm; and ~~and is used to be wirebonded thereto.~~

a circuit interconnect wirebonded to said second contact pad.

Claims 121 and 122 (canceled)

123. (previously presented) The semiconductor chip or wafer of claim 120 further comprising a polymer layer over said passivation layer, wherein said second contact pad is over said polymer layer.

Claims 124 and 125 (canceled)

126. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost nitride layer of said semiconductor chip or wafer.

127. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

128. (previously presented) The semiconductor chip or wafer of claim 120, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

129. (previously presented) The semiconductor chip or wafer of claim 120, wherein said gold layer is electroplated.

Claims 130-135 (canceled)

136. (currently amended) A circuit component comprising:

a semiconductor substrate;

a metallization structure over said semiconductor substrate;

a passivation layer over said metallization structure, wherein said passivation layer comprises an inorganic material; ~~and~~

a metal trace over said passivation layer, wherein said metal trace comprises a titanium-containing layer, a first gold layer on said titanium-containing layer, and a second gold layer on said first gold layer, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm, said first gold layer has a thickness of between 0.05 and 3 μm, and said second gold layer has a thickness of between 2 and 100 μm; and~~.~~

a circuit interconnect wirebonded to said metal trace.

Claims 137 and 138 (canceled)

139. (previously presented) The circuit component of claim 136 further comprising a polymer layer between said metal trace and said passivation layer.

140. (previously presented) The circuit component of claim 136, wherein said second gold layer is electroplated.

141. (previously presented) The semiconductor chip or wafer of claim 110, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm.

142. (previously presented) The semiconductor chip or wafer of claim 110, wherein said metal trace further comprises another gold layer between said titanium-containing layer and said gold layer, wherein said another gold layer has a thickness of between 0.05 and 3 μm.

143. (previously presented) The semiconductor chip or wafer of claim 120, wherein said second contact pad further comprises a titanium-containing layer under said gold layer.

144. (previously presented) The semiconductor chip or wafer of claim 143, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm.

145. (previously presented) The semiconductor chip or wafer of claim 143, wherein said metal trace further comprises another gold layer between said titanium-containing layer and said gold layer, wherein said another gold layer has a thickness of between 0.05 and 3 μm.

146. (previously presented) The semiconductor chip or wafer of claim 123, wherein said polymer layer has a thickness of between 2 and 50 μm.

147. (previously presented) The circuit component of claim 139, wherein said polymer layer has a thickness of between 2 and 50 μm.

148. (previously presented) The circuit component of claim 136, wherein said passivation layer comprises a topmost nitride layer of said circuit component.

149. (previously presented) The circuit component of claim 136, wherein said passivation layer comprises a topmost oxide layer of said circuit component.

150. (previously presented) The circuit component of claim 136, wherein said passivation layer comprises a topmost CVD-formed layer of said circuit component.

151. (previously presented) The circuit component of claim 136, wherein no polymer layer is over said metal trace.

152. (new) The circuit component of claim 136 further comprising a circuit interconnect wirebonded to said metal trace.

153. (new) The circuit component of claim 139, wherein said polymer layer comprises polyimide.

154. (new) The semiconductor chip or wafer of claim 106, wherein said polymer layer comprises polyimide.

155. (new) The semiconductor chip or wafer of claim 123, wherein said polymer layer comprises polyimide.